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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/926,454	11/06/2001	Syouji Higashida	107400-00044	4669

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/926,454	Applicant(s) HIGASHIDA ET AL.
	Examiner Johannes P Mondt	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 1*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al (JP410144938A) in view of Kobayashi et al (5,973,359). Yamamoto teaches a semiconductor device (cf. title) comprising:

an insulating gate field effect transistor (see [0002], first sentence) comprising a cell field 10 (see [0012], first sentence) arranged in a semiconductor layer 13 (cf. Abstract, "Solution", line 6 and Figure 1); and

a protective diode 9 (cf. Abstract, "Solution", line 1) connected between a gate and a source of said insulating gate field effect transistor to break down an input of a constant voltage or more applied between said gate and a source (see [0011], second sentence) of said insulating gate field effect transistor to break down an input of constant voltage or more applied between said gate and said source (inherent to Zener diode),

wherein said protective diode is formed as a bi-directional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers 11 and 12, respectively, (cf. [0014]) are flatly and alternately provided on an insulating layer 14 (Abstract, "Solution", line 7) at a peripheral portion of said

transistor cell field, a metal film 16 (cf. Figure 1 and Abstract, "Solution", line 9) in ring-shaped contact (cf. Figure 1 and cross-section through A-A) with the most inner layer (12 layer most to the right) and with the outer most layer (by dint: see [0003], in which it is explained that the Zener diode is formed between the gate G and source S) of said p-type layers and n-type layers, respectively, and each of said metal films is successively formed with either a source wiring or gate electrode pad consisting of a metal film, respectively (again, as explained in [0003]: the Zener diode is formed between source S and gate G).

Yamamoto does not necessarily teach the transistor to comprise a plurality of transistor cells.

However, as is evident for instance from Kobayashi et al, it is generally understood in the art of protection devices for semiconductor devices with insulated gate electrodes, such as MOS transistors, that the cell field may contain a plurality of transistor cells each protected by said Zener diode, as without any price to real estate or protection level the metal film 29 can be wired to all of the individual gates of all the transistor cells in the cell field (cf. Figure 7 and column 2, lines 24-67).

Motivation to include the teaching of Kobayashi et al in this regard in the invention taught by Yamamoto is the net reduction of the area that is needed for protection of a multi-transistor-cell field, thereby reducing complexity and cost of the device. The inventions can be *combined* in this regard, because only additional wiring is needed to protection a plurality rather than a single transistor

cell. *Success* in implementing the combination of the inventions can therefore be *reasonably expected*.

3. ***Claims 1-6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (6,268,242 B1) in view of Yamamoto (JP10144938A). Williams et al teach a semiconductor device (cf. title) comprising:

an insulating gate field effect transistor comprising a plurality of transistor cells (separated by a width W; see Figure 1) which are arranged in a semiconductor layer 108 (cf. column 3, lines 39-40) and connected in parallel; and

a protective diode D1 (and D2) (cf. column 3, lines 58-64) connected between a gate and a source of said insulating gate field effect transistor to break down an input of a constant voltage or more applied between said gate and said source (inherent in diode), wherein said protective diode is formed as a bi-directional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers 130 (cf. column 3, lines 58-64) are flatly and alternately provided on an insulating layer 132 (cf. column 3, line 60) at a peripheral portion of said transistor cells, metal films 112 and 134 (cf. column 3, line 62) (cf. Figures 7A and 7B) contacting with the innermost and outermost layer of said p-type layers or said n-type layers are formed respectively, and each of said metal films is successively formed with either of a source wiring (namely: 112) or a gate electrode pad consisting of a metal film (namely: 134), respectively.

Williams does not necessarily teach the metal film contacting of the innermost and outermost layers also to be ring-shaped. However, it would have been obvious to improve the invention by Williams to include such ring-shaped contacts in view of Yamamoto, who teaches for the specific purpose of increasing the electrostatic strength of a Zener diode that said Zener diode and its contact metal be formed so as to encircle the cell region (see Abstract, "Problem to be Solved", first sentence).

Motivation to include the teaching in this regard by Yamamoto is the consequent improvement of the capability of the Zener diode to protect against electrostatic discharge. The inventions can be *combined* in this regard, because the contact area between the inner – and outermost Zener diode p-type or n-type layers with the metal films can easily be extended to form a ring, as evidenced by the plan view of the invention by Williams (see Figure 7B). *Success* of the implementation of this combination can therefore be *reasonably expected.*

With regard to claim 2: in the semiconductor device by Williams when improved by making the metal films ring-shaped as taught by Yamamoto in the manner discussed above in connexion with claim 1, one metal ring-shaped metal film of said metal films is provided so as to contact with said most outer layer is a gate wiring successively formed with said gate electrode pad (134; cf. Figure 1), and the other metal film of said metal films is provided so as to contact the most inner layer is said source wiring (112; cf. Figure 1). See also Figure 7B.

With regard to claim 3: the one ring-shaped metal film as essentially taught in the above-defined combination of the inventions by Williams et al and Yamamoto is a gate wiring 712 which has gate connecting portions so as to connect to gate electrodes of said transistor cells with partial striding over said protective diode in polysilicon layer 706 (cf. Figure 7A and column 10, line 1), and said gate connecting portions and source connecting portions of said source wiring which are contacted with said most inner layer are alternately formed in plan view (cf. Figure 7B).

With regard to claim 4: the p-type and n-type layers in the above-defined combination of the inventions by Williams et al and Yamamoto are made of polysilicon (cf. column 3, lines 58-63 and column 9, line 67 – column 10, line 1).

With regard to claim 5: although neither Williams et al nor Yamamoto necessarily teach the further limitation as defined by claim 5, it is understood in the art of semiconductor devices that the subsequent portions of the same conductivity type in the Zener diode, when having roughly the same width and the same impurity concentration, have approximately the same electrostatic breakdown properties so that the electrostatic load be about evenly divided, which is a reasonable choice. However, there is no compelling reason, why the above-mentioned ranges for the ratio of (a) width (around 1) and (b) impurity concentrations (around 1) is critical to the invention of Applicant, nor does Applicant show such criticality. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering

the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to claim 6: the semiconductor device as taught by Williams et al in view of Yamamoto has a diffusion region of P+ conductivity type formed on the closest side to said protective diode of said transistor cells arranged (therein), namely the P+ region abutting region 110A (cf. column 3, line 50 and column 3, lines 35-48) in Figure 1, and said source wiring 112 contacting the innermost layer of said protective diode is contacted (is in direct contact) with said P+ region (see Figure 1).

4. ***Claim 7*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al and Yamamoto, or, in the alternative, over Yamamoto and Kobayashi et al as applied to claim 1 above, and further in view of Throngnumchai et al (4,963,970). As detailed above, claim 1 is unpatentable over Yamamoto in view of Kobayashi et al, or, in the alternative, over Williams et al in view of Yamamoto. Yamamoto, Kobayashi et al nor Williams et al necessarily teach the further limitation as defined by claim 7. However, electrostatic protection of an insulated gate field effect device, particularly as vertical MOSFET device, through a vertically stacked Zener diode, with one innermost or upper p-type layer wired to the source and one outermost or lower n-type layer wired to the gate has long been known in the semiconductor device ESD protection art, as witnessed by Throngnumchai et al, who teach a vertical MOSFET with a Zener diode not flatly formed but instead alternately formed in a height direction, specifically: p-type layer 39 wired to the source S and n-type region 37 wired to the gate G (see Figure 3 ,

abstract, and column 2, lines 28-56). *Motivation* to include the teaching in this regard by Throngnumchai et al in the invention essentially taught by Yamamoto and Kobayashi et al, or, in the alternative, in the invention essentially taught by Williams et al and Yamamoto, stems from the obvious savings in lateral real estate by stacking said p-type and n-type layers vertically rather then laterally. The inventions can be easily *combined* by changing the direction of stacking without any consequence to the remainder of the aforementioned inventions. *Success* of the implementation of the combination can therefore be *reasonably expected*.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
October 3, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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